

1. Features

- Built-in $6m\Omega$ 50V MOSFET
- High efficiency and low case temperature
- Fewer external components

2. Applications

- Smart phone chargers
- 5V adapters

3. Typical applications (5V/3.3A charger)

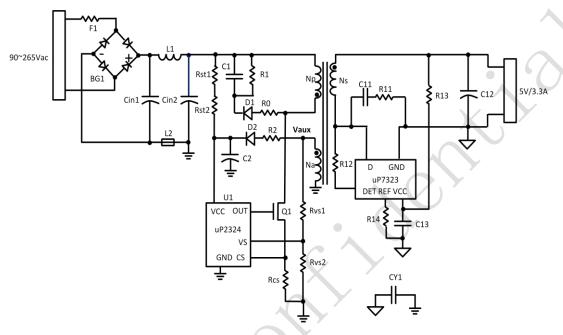
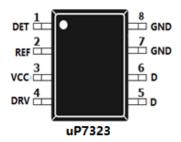


Fig.1 Typical applications

4. Pin definitions



μΡ7323	Pin Name	Pin Type	Pin Functions
1	DET	Input	Drain voltage detection of SR MOSFET
2	REF	Output	Voltage setting for SR MOSFET turn on
3	VCC	Power supply	Power supply of the rectifier
4	DRV	Output	Gate drive of SR MOSFET
5,6	D	Input/Output	Drain of SR MOSFET
7,8	GND	Ground	



5. Absolute maximum ratings (Note 1)

Parameter	Name	Range	Unit
Voltage at VCC to Ground	VCC	-0.3 to 6.5	V
Voltage at DRV to Ground	DRV	-0.3 to 6	V
Voltage at DET to Ground	DET	-2 to 50	V
Voltage at D to Ground	D	-2 to 50	V
Voltage at REF to Ground	REF	-0.3 to 6	V
Power dissipation @ T _A =25 °C	P_D	0.5	W
Maximum junction temperature	Тумах	150	\mathcal{C}
Lead temperature	TLEAD	300	\mathcal{L}
Storage temperature	Tstg	-55 to 150	$\mathcal C$
ESD rating per ANSI/STM5.1-2001	HBM	2000	V
ESD rating per JEDEC JESD22-C101F	CDM	1000	V
Latchup test per JEDEC 78D		+/-200	mA

Note1: Stresses over those listed under "Absolute maximum ratings" may cause permanent damages to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to "Absolute Maximum Ratings" for extended periods of time may affect device reliability.

6. Thermal parameter

Junction to ambient thermal resistance	θ JA(SOP8)	90	°C/W
Junction to case thermal resistance	θ JC(SOP8)	45	°C/W

7. Recommended operating conditions

Parameter	Symbol	Min	Max	Unit	
Supply voltage	VCC	3.3	6	V	
Ambient Temperature	TA	-40	85	${\mathcal C}$	

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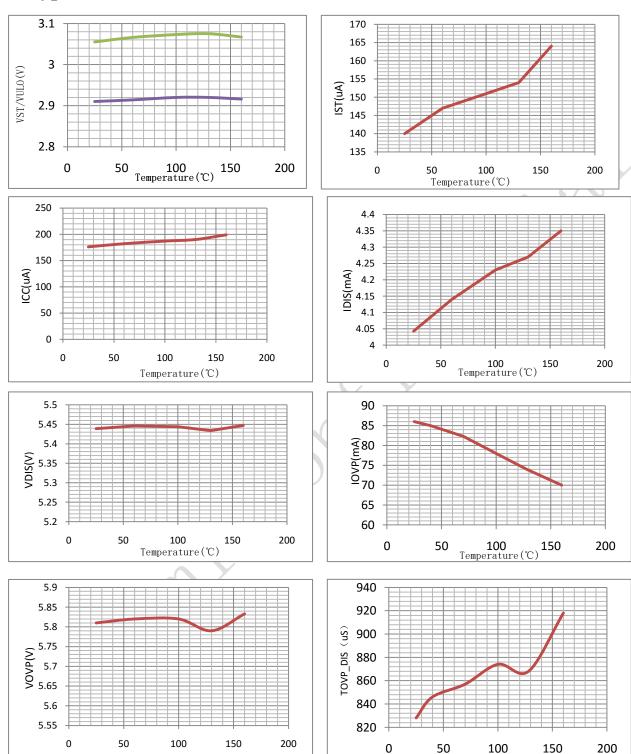
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8. Electrical parameters (TA = 25 $^{\circ}$ C, unless otherwise specified)

Parameter	Symbol	Condition	Min	Тур	Max	Unit
Power supply(VCC pin)						
Operating current	Icc		170	200	230	μΑ
Startup voltage	Vst		2.67	2.98	3.29	V
Minimum operating voltage	Vuvlo		2.49	2.80	3.11	V
Startup current	Ist	VCC= Vst -0.1V	110	150	170	μΑ
Output voltage monitor					\bigcirc	5
Output low voltage	Vtrg		5.24	5.30	5.36	V
VCC discharge voltage	VDIS		5.38	5.47	5.56	V
VCC discharge current	Idis	VCC= V _{DIS} +0.1V	. (4	6	mA
VCC protection voltage	$V_{ ext{OVP}}$		5.74	5.85	5.96	V
VCC over voltage discharge current	Iovp	VCC= Vovp+0.1V	39	85	131	mA
VCC OVP discharge time	Tovpdis			80		μS
Internal oscillator period	Tosc	X	20	25	30	μS
Synchronous rectification con	ntrol	Y				
SR turn on voltage	VTHON			75		mV
SR turn off voltage	VTHOFF		-6	-4	2	mV
SR turn on delay time	TDON			70	130	nS
SR turn off delay time	TDOFF			100	150	nS
SR turn on rising time	Tr	C _L =4.7nF		50	100	nS
SR turn on falling time	Tr	C _L =4.7nF		50	100	nS
SR minimum on time	TLEB_S	(V _{DET} -VCC)*T _{ONP} =30V*µS		2.2		μS
SR minimum operating voltage(V _{DET} -VCC)	V _{S_MIN}	Minimum DET pin voltage@VCC=5V		3.0		V
Ampere Second Product	ASP	(V _{DET} -VCC)*T _{ONP} =25V*µS	0.5	0.7	0.9	mA*μS
SR MOSFET characteristics						
Drain to source breakdown	BVdss		50			V
Gate threshold voltage	$V_{\text{GS(TH)}}$	$V_{DS} = V_{GS}$, $I_D = 0.25 \text{mA}$	1.2	1.8	2.5	V
Static Drain-to-Source On Resistance(μP7323C)	Rdson	$V_{GS}=5.5V$, $I_{D}=10A$		6	8	mΩ
Drain-to-Source leakage	Idss	$V_{GS}=0V$, $V_{DS}=50V$			1	μΑ
Gate to source leakage	Igss	V _{GS} =+/-20V	-100		100	nA



9. Typical Characteristics

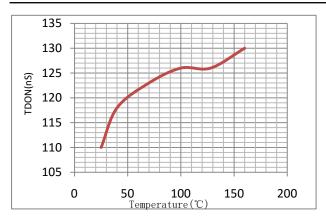


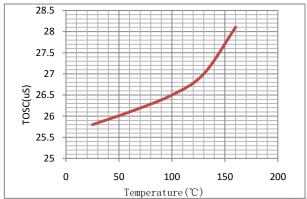
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Temperature(℃)

Temperature(°C)







10. Functional block diagram

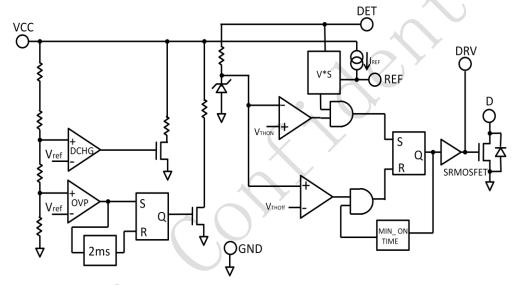


Fig.2, μP7323 block diagram

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11. Principle of operation

The μ P7323 has two major functions: output voltage monitor (discharge of output capacitor at certain conditions) and synchronous rectification. The device must work in Discontinuous Conduction Mode (DCM).

11.1 Power up and power down sequences

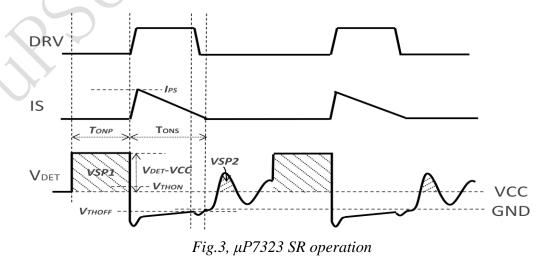
Refer to Fig.1 and Fig.2, after AC power supply is applied to the converter, the primary controller μ P2324 (U1) starts to deliver energy to the output capacitor C12, the output voltage begins rising from 0V.

When the VCC voltage of μ P7323 (U2) is lower than the startup voltage VsT, the synchronous rectifier does not work, the body diode of the SR MOSFET acts as the rectification diode, with around -1.5V forward conduction voltage since the body diode of the SRMOSFET is just an ordinary PN junction.

When the VCC voltage of $\mu P2323(U2)$ is larger than the startup voltage VsT, the synchronous rectifier starts to work, as described in 10.4. When the AC power supply is removed from the converter, the VCC voltage of $\mu P7323$ (U2) falls below Vuvlo, the synchronous rectifier stops working, the body diode of the SRMOSFET acts again as the rectification diode.

11.2 Discharge of output capacitor

When the VCC voltage of $\mu P7323$ (U2) is higher than a specified voltage Vdis, $\mu P7323$ will turn on a discharge path from VCC to GND with typical 3mA current capacity to make the system output voltage stay around Vdis. When the VCC voltage of $\mu P7323$ (U2) is further higher than a specified voltage Vovp, such as in case of load transient from full load to no load, $\mu P7323$ will turn on another discharge path from VCC to GND with typical 70mA current capacity to limit the system output over shoot voltage.





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11.3 Synchronous rectification

Refer to Fig3, μ P7323 monitors the SR MOSFET drain to source voltage at DET pin. When the V_{DET} is lower than the turn-on threshold voltage V_{THON}, μ P7323 DRV pin generates a positive drive voltage after a turn-on delay time (T_{DON}). The SR MOSFET will turn on and the current will transfer from the body diode to the channel of the SR MOSFET.

After the conduction of the SR MOSFET, the V_{DET} rises linearly. When it rises over the turn off threshold voltage V_{THOFF}, μP7323 DRV pin generates a pull down signal after a turn-off delay (T_{DOFF}).

During the SRMOSFET turn on process, some ringing noise may be generated. The minimum on-time block blanks the output of V_{THOFF} comparator, keeping the SR MOSFET on for at least the minimum on time. The minimum on time is proportional to the volt second product (VSP) of the primary side power switch on state, which is equal to $(V_{DET}-VCC)*T_{ONP}$. Given $(V_{DET}-VCC)*T_{ONP}$ =25V* μ S, the minimum on time is about 1.8 μ S.

As the convertor operates in DCM, after synchronous rectifier stops conduction, resonant ringing is resulted due to the primary inductance and power switch parasitic capacitance. This ringing waveform may leads to the error conduction of the synchronous rectifier.

To avoid this fault, $\mu P7323$ judges the primary power switch turn on by the Volt-Second Product (VSP) of the system. The volt-second product (VSP1) of a primary switch turn on is much higher than the volt-second product (VSP2) of the resonant ringing waveform, as illustrated in Fig.3. Thus, before to turn on the synchronous rectifier, $\mu P7323$ judges if the detected volt-second product of VDET voltage above VCC is higher than a threshold (VSPREF) and then turn on synchronous rectifier if the detected VSP is larger than VSPREF. The purpose of REF resistor is to set the volt-second product threshold (VSPREF). The detected volt-second product

$$VSP = \int (V_{DET}-VCC)*dt = Rv_{SP}*Cv_{SP}*V_{VSP}$$

Where R_{VSP} is an internal resistor to convert the (V_{DET} -VCC) voltage to charge an internal capacitor C_{VSP} , and V_{VSP} is the voltage rise on C_{VSP} when the charging phase is completed. In $\mu P7323$, the V_{VSP} judges whether the VSP is generated by primary side power switch or not is set by an internal current source I_{REF} and outside resistor R_{REF} (R14 in Fig.1). So, the judging volt-second product

$$VSP_{REF} = (R_{VSP} * C_{VSP} * I_{REF}) * R_{REF} = ASP * R_{REF}$$

Where ASP=($R_{VSP}*C_{VSP}*I_{REF}$) is an $\mu P7323$ determined "Ampere Second Product" to set system VSP_{REF} with R_{REF} . VSP_{REF} depends on system design and are always fixed after system design is frozen. R_{REF} resistor should be considered for the worst case, that is, the minimum primary peak current condition. VSP_{REF} should be designed in the middle of VSP1 and VSP2.

 μ P7323 also sets a minimum line voltage to operate the SR MOSFET. The value of V_{DET}–VCC during primary side power switch turn on time (T_{ONP}) must be higher than V_{S_MIN} to enable the



synchronous rectifier. That is, the minimum rectified input line voltage (V_{IN_MIN}) to enable the SR is $V_{IN_MIN} = (V_{DET} - VCC)*(N_P/N_S)$

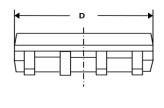


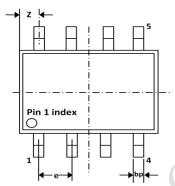
12. Ordering information

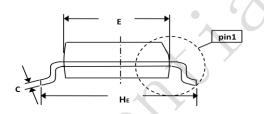
Part number	Package	Marking ID	Packing	Output power	
μΡ7323	SOP8	7323M	3000 / Reel	15W~20W	

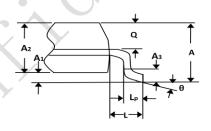
13. Mechanical dimensions

SOP8









UNIT	A	A1	A2	A3	bp	с	D	Е	e	HE	L	Lp	Q	θ
mm	1.75	0.1/ 0.25	1.25/ 1.5	0.25	0.33/ 0.51	0.19/ 0.25	<i>4.7/ 5.1</i>	3.8/ 4.0	1.27	5.8/ 6.2	1.05	0.4/ 1.0	0.6/ 0.7	8°