

#### 1. Features

- Built-in 18mΩ on-resistance and 45V breakdown voltage MOSFET
- Programmable resistor to filter resonant ringing signals
- Fewest components counts

• Excellent system ESD and EFT performance

## 2. Applications

- Smart phone chargers
- Power strip with USB ports
- 5V adapters

## 3. Typical applications (5V/2.4A charger)

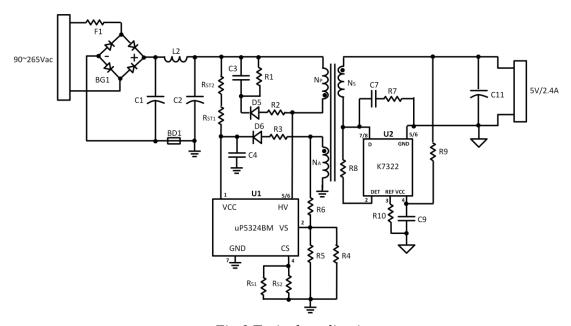
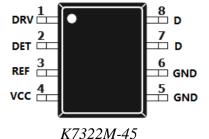


Fig.1 Typical applications

### 4. Ordering information

Part number	Mark ID	Package	Quantity per reel	Output power
K7322M-45	7322M-45	SOP-8	3,000	10~12W

### 5. Pin definitions



Pin Name	Pin Type	Pinout	Pin Functions
DRV	Output	1	Gate drive of SR MOSFET
DET	Input	2	Drain voltage detection of SR MOSFET
REF	Output	3	Volt-second setting for SR MOSFET turn on
VCC	Power supply	4	Power supply of the rectifier



GND	Ground	5, 6	Source of the SR MOSFET and the power ground.
D	Drain	7, 8	Drain of the SR MOSFET

### 5. Absolute maximum ratings (*Note 1*)

Parameter	Name	Range	Unit
Voltage range	VCC	-0.3 to 7	V
Voltage range	DRV	-0.3 to 6	V
Voltage range	DET	-2 to 50	V
Voltage range	REF	-0.3 to 6	V
Voltage range	D	-2 to 45	V
Continuous drain current	$I_D$	10	A
Pulse drain current	$I_{DP}$	40	A
Power dissipation @ $T_A=25  \mathrm{C}$	$P_D$	0.8	W
Maximum junction temperature	$T_{JMAX}$	150	$\mathcal C$
Lead temperature	$T_{LEAD}$	300	${\mathcal C}$
Storage temperature	$T_{STG}$	-55 to 150	$\mathcal{C}$
ESD rating per JEDEC JESD22-A114	HBM	2000	V
ESD rating per JEDEC JESD22-C101C	CDM	1000	V
Latchup test per JEDEC 78		+/-200	mA

Note1: Stresses over those listed under "Absolute maximum ratings" may cause permanent damages to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to "Absolute Maximum Ratings" for extended periods of time may affect device reliability.

### 6. Thermal parameter

Junction to ambient thermal resistance	<b>θ</b> JA(SOP-8)	90	C/W
Junction to case thermal resistance	<b>Ө</b> <i>JC</i> (SOP-8)	45	℃/W

## 7. Recommended operating conditions

Parameter	Symbol	Min	Max	Unit
Supply voltage	VCC	3.3	6	V
Ambient Temperature	$T_A$	-40	85	${\mathcal C}$

## 8. Electrical parameters

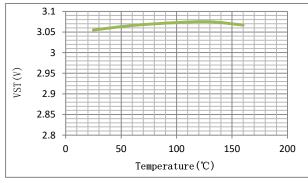
#### $T_A = 25 \, \text{C}$ , unless otherwise specified

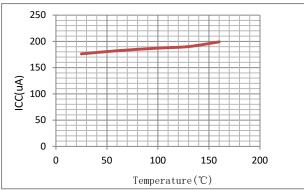
Parameter	Symbol	Condition	Min	Тур	Max	Unit				
Power supply(VCC pin)										
Operating current	Icc		180	200	220	$\mu A$				
Startup voltage	VsT		2.68	2.98	3.28	V				
Minimum operating voltage	Vuvlo		2.5	2.8	3.1	V				
Startup current	<b>I</b> ST	VCC = Vst - 0.1V	110	140	170	$\mu A$				
Output voltage monitor										
VCC discharge voltage	VDIS		5.39	5.47	5.55	V				
VCC discharge current	IDIS	$VCC = V_{DIS} + 0.1V$	1.5	3	4.5	mA				

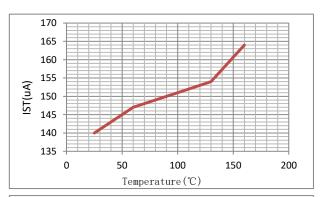


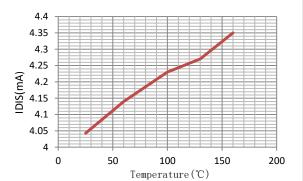
## Preliminary Datasheet 1.2

VCC protection voltage	$V_{\it OVP}$		5.75	5.85	5.95	V	
VCC over voltage discharge	Iovp	$VCC = V_{OVP} + 0.1V$	40	97	130	mA	
current	TOVP	VCC= VOVP+0.1V	40	97	130	ША	
VCC OVP discharge time	$T_{OVPDIS}$		672	800	928	$\mu S$	
Internal oscillator period	Tosc		21	25	29	μS	
Synchronous rectification con	ntrol						
SR turn on voltage	VTHON			75		mV	
SR turn off voltage	VTHOFF		-6	-2	2	mV	
SR turn on delay time	TDON		10	70	130	nS	
SR turn off delay time	Tooff		10	100	150	nS	
SR turn on rising time	$T_R$	$C_L=4.7nF$	10		100	nS	
SR turn off falling time	$T_F$	$C_L=4.7nF$	10		100	nS	
SR minimum on time	TLEB_S	$(V_{DET}-VCC)*T_{ONP}$ $=30V*\mu S$		2.2		μS	
SR minimum operating voltage(VDET-VCC)	V <sub>S_MIN</sub>	Minimum DET pin voltage@VCC=5V		3.0		V	
Ampere Second Product	ASP	$(V_{DET}-VCC)*T_{ONP}$ $=25V*\mu S$	0.5	0.7	0.9	mA*μS	
SR MOSFET characteristics							
Drain to source breakdown	BVdss	$V_{GS}=0V, I_{D}=0.25mA$	45			V	
Gate threshold voltage	$V_{\it GS(TH)}$	$V_{DS} = V_{GS},$ $I_D = 0.25 mA$	1.0	1.5	2.0	V	
Static Drain-to-Source On Resistance	$R_{DSON}$	$V_{GS}=5.5V$ , $I_D=15A$		18	25	$m\Omega$	
Drain-to-Source leakage	$I_{DSS}$	$V_{GS}=0V$ , $V_{DS}=50V$			1	$\mu A$	
Gate to source leakage	$I_{GSS}$	$V_{GS} = +/-20V$	-100		100	пA	





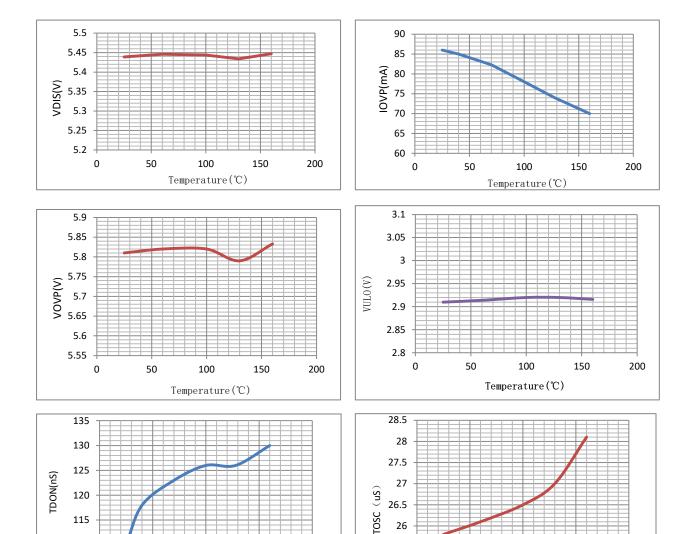




150

Temperature(℃)





# 9. Functional block diagram

100

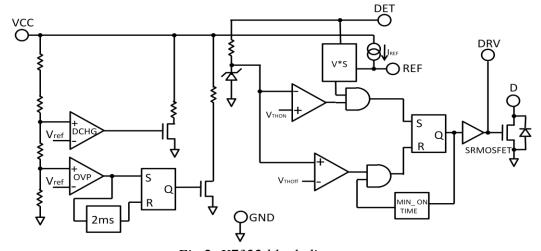
Temperature(℃)

150

200

110

105



25.5 25

Fig.2, K7322 block diagram

### 10. Principle of operation

The K7322 has two major functions: output voltage monitor to discharge output capacitor at certain conditions and synchronous rectification. The device must work in Discontinuous Conduction Mode (DCM) or Quasi-Resonant Mode (QRM).

#### 10.1 Power up and power down sequences

Refer to Fig.1 and Fig.2, after AC power supply is applied to the converter, the primary controller UP5324A (U1) starts to deliver energy to the output capacitor C11, the output voltage begins rising from 0V. When the VCC voltage of K7322 (U2) is lower than the startup voltage Vst, the synchronous rectifier does not work, the body diode of the SR MOSFET acts as the rectification diode, with around -1.5V forward conduction voltage since the body diode of the SRMOSFET is just an ordinary PN junction. When the VCC voltage of K7322 (U2) is larger than the startup voltage Vst, the synchronous rectifier starts to work, as described in 10.3. When the AC power supply is removed from the converter, the VCC voltage of K7322 (U2) falls below Vvvlo, the synchronous rectifier stops working, the body diode of the SRMOSFET acts again as the rectification diode.

#### 10.2 Discharge of output capacitor

When the VCC voltage of K7322 (U2) is higher than a specified voltage Vdis, K7322 will turn on a discharge path from VCC to GND with typical 3mA current capacity to make the system output voltage stay around Vdis. When the VCC voltage of K7322 (U2) is further higher than a specified voltage Vovp, such as in case of load transient from full load to no load, K7322 will turn on another discharge path from VCC to GND with typical 70mA current capacity to limit the system output over shoot voltage.

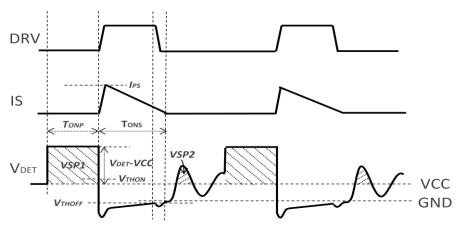


Fig.3, K7322 SR operation

#### 10.3 Synchronous rectification

Refer to Fig3, K7322 monitors the SR MOSFET drain to source voltage at DET pin. When the V<sub>DET</sub> is lower than the turn-on threshold voltage V<sub>THON</sub>, K7322 DRV pin generates a positive drive voltage after a turn-on delay time (T<sub>DON</sub>). The SR MOSFET will turn on and the current will transfer from the body diode to the channel of the SR MOSFET.

After the conduction of the SR MOSFET, the V<sub>DET</sub> rises linearly. When it rises over the turn off threshold voltage V<sub>THOFF</sub>, K7322 DRV pin generates a pull down signal after a turn-off delay (T<sub>DOFF</sub>).

During the SRMOSFET turn on process, some ringing noise may be generated. The minimum on-time block blanks the output of  $V_{THOFF}$  comparator, keeping the SR MOSFET on for at least the

minimum on time. The minimum on time is proportional to the volt second product (VSP) of the primary side power switch on state, which is equal to  $(V_{DET}-VCC)*T_{ONP}$ . If  $(V_{DET}-VCC)*T_{ONP}$  =  $30V*\mu S$ , the minimum on time is about  $2.2\mu S$ .

As the convertor operates in DCM or QRM, after synchronous rectifier stops conduction, resonant ringing is resulted due to the primary inductance and power switch parasitic capacitance. This ringing waveform may leads to the error conduction of the synchronous rectifier. To avoid this fault, K7322 judges the primary power switch turn on by the Volt-Second Product (VSP) of the system. The volt-second product (VSP1) of a primary switch turn on is much higher than the volt-second product (VSP2) of the resonant ringing waveform, as illustrated in Fig.3. Thus, before to turn on the synchronous rectifier, K7322 judges if the detected volt-second product of VDET voltage above VCC is higher than a threshold (VSPREF) and then turn on synchronous rectifier if the detected VSP is larger than VSPREF. The purpose of REF resistor is to set the volt-second product threshold (VSPREF). The detected volt-second product

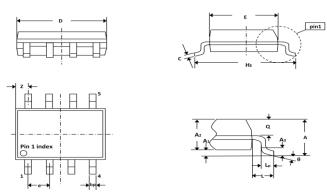
$$VSP = \int (V_{DET} - VCC) * dt = R_{VSP} * C_{VSP} * V_{VSP}$$

Where  $R_{VSP}$  is an internal resistor to convert the ( $V_{DET}$ -VCC) voltage to charge an internal capacitor  $C_{VSP}$ , and  $V_{VSP}$  is the voltage rise on  $C_{VSP}$  when the charging phase is completed. In K7322, the  $V_{VSP}$  to judge whether the VSP is generated by primary side power switch or not is set by an internal current source  $I_{REF}$  and outside resistor  $R_{REF}$  ( $R_{ID}$  in Fig.1). So, the judging volt-second product  $VSP_{REF} = (R_{VSP} * C_{VSP} * I_{REF}) * R_{REF} = ASP * R_{REF}$ 

Where ASP=(Rvsp\*Cvsp\*Iref) is a K7322 determined "Ampere Second Product" to set system VSPref with Rref. VSPref depends on system design and are always fixed after system design is frozen. Rref resistor should be considered for the worst case, that is, the minimum primary peak current condition. VSPref should be designed in the middle of VSP1 and VSP2. K7322 also sets a minimum line voltage to operate the SR MOSFET. The value of VDET-VCC during primary side power switch turn on time (TONP) must be higher than Vs\_min to enable the synchronous rectifier. That is, the minimum rectified input line voltage (Vin\_min) to enable the SR is

$$V_{IN\_MIN} = V_{S\_MIN} * (N_P/N_S)$$

#### 11. Mechanical dimensions



UNIT	A	A1	A2	A3	bp	с	D	E	e	HE	L	Lp	Q	θ
mm	1.75	0.1/ 0.25	1.25/ 1.5	0.25	0.33/ 0.51	0.19/ 0.25	<i>4.7/ 5.1</i>	3.8/ 4.0	1.27	5.8/ 6.2	1.05	0.4/ 1.0	0.6/ 0.7	8°