

#### 1. Features

- Built-in 10mΩ 50V MOSFET
- Support various kind of primary side controller in DCM or QR mode
- Excellent system ESD performance

- Enhanced undershoot performance
- Tight control of SR turnoff timing

### 2. Applications

- Smart phone chargers
- 5V adapters

# 3. Typical Applications (5V/3A charger)

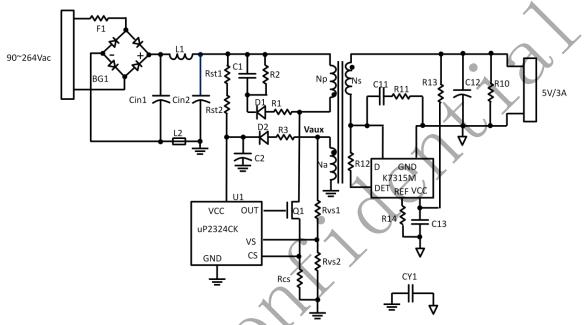
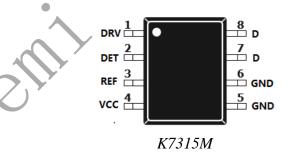


Fig.1 Typical Applications of K7315M

#### 4. Pin Definitions



K7315	Pin Name	Pin Type	Pin Functions
1	DRV	Output	Gate drive of SR MOSFET
2	DET	Input	Drain voltage detection of SR MOSFET
3	REF	Output	Volt-second setting for SR MOSFET turn on
4	VCC	Power supply	Power supply of the rectifier
5,6	GND	Ground	Source of SR MOSFET
7,8	D	Input/Output	Drain of SR MOSFET



### **5. Absolute Maximum Ratings** (Note 1)

Parameter	Name	Range	Unit
Voltage at VCC to Ground	VCC	-0.3 to 7	V
Voltage at DRV to Ground	DRV	-0.3 to 6	V
Voltage at DET to Ground	DET	-2 to 50	V
Voltage at D to Ground	D	-2 to 50	X
Voltage at REF to Ground	REF	-0.3 to 6	V
Power Dissipation @ T <sub>A</sub> =25 °C	$P_{D}$	0.7	W
Maximum Junction Temperature	Тлмах	150	$\mathcal{C}$
Lead Temperature	TLEAD	300	$\mathcal{C}$
Storage Temperature	Tstg	-55 to 150	$\mathcal C$
ESD rating per ANSI/STM5.1-2001	HBM	2000)	V
ESD rating per JEDEC JESD22-C101F	CDM •	1000	V
Latchup test per JEDEC 78D	C	+/-200	mA

Note1: Stresses over those listed under "Absolute maximum ratings" may cause permanent damages to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to "Absolute Maximum Ratings" for extended periods of time may affect device reliability.

#### **6. Thermal Parameter** (Note 2)

Junction to Ambient Thermal Resistance	θ ja(SOP8)	170	℃/W
Junction to Case Thermal Resistance	<b>θ</b> јс(SOP8)	25	°C/W

Note2: FR-4 substrate PC board, 2oz copper, with 1 inch square pad layout.

## 7. Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage	VCC	3.3	6	V
Ambient Temperature	TA	-40	85	$\mathcal C$

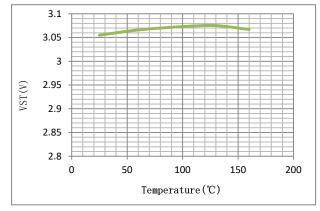


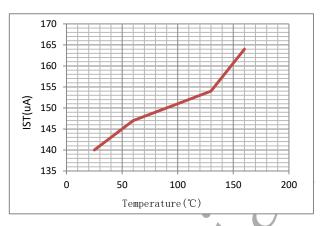
# **8. Electrical Parameters** (TA =25 °C, unless otherwise specified)

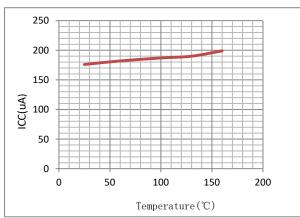
Parameter	Symbol	Condition	Min	Тур	Max	Unit
Power Supply(VCC pin)						
Operating Current	Icc		170	210	250	μΑ
Startup Voltage	Vst		2.75	3.10	3.45	V
Minimum Operating Voltage	Vuvlo		2.65	3.00	3.35	V
Startup Current	Ist	VCC= Vst -0.1V	120	160	200	μA
<b>Output Voltage Monitor</b>						
Output Low Voltage	Vtrg		5.15	5.20	5.25	V
VCC Discharge Voltage	Vdis		5.27	5.36	5.45	V
VCC Discharge Current	Idis	VCC= Vdis+0.1V	1.4	4	5	mA
VCC Protection Voltage	V <sub>OVP</sub>		5.62	5.73	5.84	V
VCC Over Voltage Discharge Current	Iovp	VCC= Vovp+0.1V	39	65	131	mA
VCC OVP Discharge Time	Tovpdis		50	80	130	μS
Internal Oscillator Period	Tosc	$C \wedge$	20	25	30	μS
<b>Synchronous Rectification</b>	Control	X				
SR Turn On Voltage	VTHON	Y		75		mV
SR Turn Off Voltage	VTHOFF		-6	-4	2	mV
SR Turn On Delay Time	Toon			70		nS
SR Turn Off Delay Time	TDOFF			100		nS
SR Turn On Rising Time	TR	$C_L=4.7nF$		50	100	nS
SR Turn On Falling Time	TR	$C_L=4.7nF$		100	150	nS
SR Minimum On Time	TLEB_S	$(V_{\text{DET}}\text{-}VCC)^*T_{\text{ONP}} = 30V^*\mu S$		2.2		μS
SR Minimum Operating Voltage(VDET-VCC)	V <sub>S_MIN</sub>	Minimum DET pin voltage@VCC=5V		3.0		V
Ampere Second Product	ASP	$(V_{\text{DET}}\text{-}VCC)^*T_{\text{ONP}} = 25V^*\mu S$	0.5	0.7	0.9	mA*μS
SR MOSFET Characterist	tics					
Drain to Source Breakdown	BVdss		50			V
Gate Threshold Voltage	$V_{\text{GS(TH)}}$	$V_{DS} = V_{GS}$ , $I_D = 0.25 \text{mA}$	1.2	1.8	2.5	V
Static Drain-to-Source On Resistance	Rdson	$V_{GS}=5.5V$ , $I_{D}=10A$		10		mΩ
Drain-to-Source Leakage	Idss	$V_{GS}=0V$ , $V_{DS}=50V$			1	μΑ
Gate to Source Leakage	Igss	$V_{GS}=+/-20V$	-100		100	nA

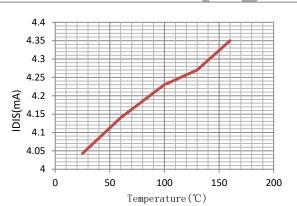


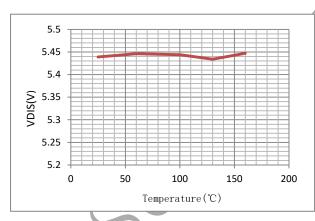
## 9. Typical Characteristics

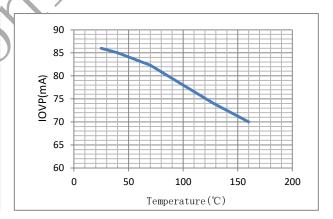


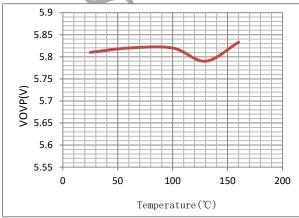


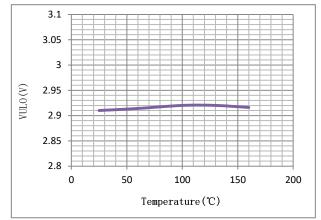




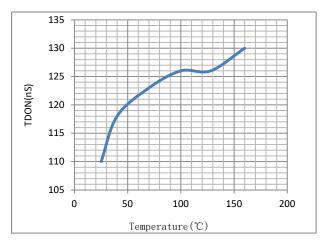


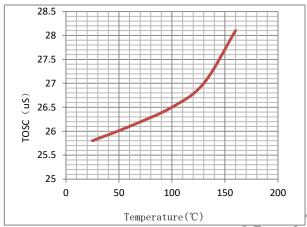












## 10. Functional Block Diagram

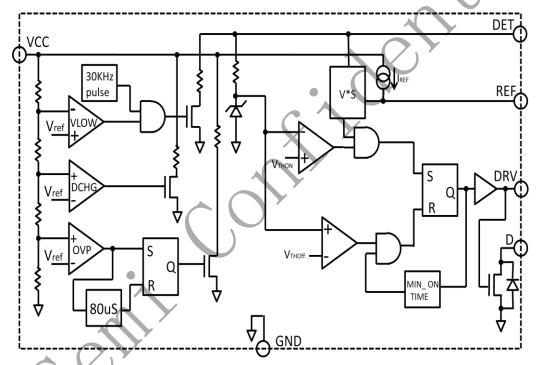


Fig.2, K7315M block diagram



## 11. Principle of Operation

The K7315 has two major functions: output voltage monitor (discharge of output capacitor at certain conditions, etc.) and synchronous rectification control. The device must work in Discontinuous Conduction Mode (DCM) or Quasi-Resonant (QR) mode.

#### 11.1 Power Up and Power Down Sequences

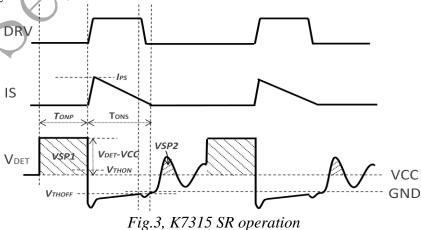
Refer to Fig.1 and Fig.2, after AC power supply is applied to the converter, the primary side controller  $\mu$ P2324 (U1) starts to deliver energy to the output capacitor C12, the output voltage begins rising from 0V.

When the VCC voltage of K7315 (U2) is lower than the startup voltage VsT, the synchronous rectifier does not work, the body diode of the SR MOSFET acts as the rectification diode, with around -1.5V forward conduction voltage since the body diode of the SRMOSFET is just an ordinary PN junction.

When the VCC voltage of K7315 (U2) is larger than the startup voltage VsT, the synchronous rectifier starts to work, as described in 11.3. When the AC power supply is removed from the converter, the VCC voltage of K7315 (U2) falls below Vuvlo, the synchronous rectifier stops working, the body diode of the SRMOSFET acts again as the rectification diode.

#### 11.2 Discharge of Output Capacitor

When the VCC voltage of K7315 (U2) is higher than a specified voltage Vdis, K7315 will turn on a discharge path from VCC to GND with typical 3mA current capacity to make the system output voltage stay around Vdis. When the VCC voltage of K7315 (U2) is further higher than a specified voltage Vove, such as in case of load transient from full load to no load, K7315 will turn on another discharge path from VCC to GND with typical 70mA current capacity to limit the system output over shoot voltage.



### 11.3 Synchronous Rectification

## K7315M

### Synchronous Rectifier



Refer to Fig2, K7315M monitors the SR MOSFET drain to source voltage at DET pin. When the V<sub>DET</sub> is lower than the turn-on threshold voltage V<sub>THON</sub>, K7315M DRV pin generates a positive drive voltage after a turn-on delay time (T<sub>DON</sub>). The SR MOSFET will be turned on and the secondary winding current will flow in the channel of the SR MOSFET.

After the conduction of the SR MOSFET, the V<sub>DET</sub> rises linearly. When it rises over the turn off threshold voltage V<sub>THOFF</sub>, K7315M DRV pin generates a pull down signal after a turn-off delay (T<sub>DOFF</sub>).

During the SR MOSFET turn on process, some ringing noise may be generated. The minimum on-time block blanks the output of  $V_{THOFF}$  comparator, keeping the SR MOSFET on for at least the minimum on time. The minimum on time is proportional to the volt second product (VSP) of the primary side power switch on state, which is equal to  $(V_{DET}-VCC)*T_{ONP}$ . If  $(V_{DET}-VCC)*T_{ONP}=30V*\mu S$ , the minimum on time is about  $2.2\mu S$ .

As the convertor operates in DCM or QR mode, after synchronous rectifier stops conducting, resonant ringing is resulted due to the primary inductance and power switch parasitic capacitance. This ringing waveform may leads to the error conduction of the synchronous rectifier.

To avoid this fault, K7315M judges the primary power switch turn on by the Volt-Second Product (VSP) of the system. The volt-second product (VSP1) of a primary switch turn on is much higher than the volt-second product (VSP2) of the resonant ringing waveform, as illustrated in Fig.3. Thus, before to turn on the synchronous rectifier, K7315M judges if the detected volt-second product of V<sub>DET</sub> voltage above VCC is higher than a threshold (VSP<sub>REF</sub>). If the detected VSP is larger than VSP<sub>REF</sub>, K7315M will turn on the synchronous rectifier. The purpose of REF resistor is to set the volt-second product threshold (VSP<sub>REF</sub>). The detected volt-second product

$$VSP = \int (V_{DET} - VCC) * dt = R_{VSP} * C_{VSP} * V_{VSP}$$

Where  $R_{VSP}$  is an internal resistor to convert the ( $V_{DET}$ -VCC) voltage to charge an internal capacitor  $C_{VSP}$ , and  $V_{VSP}$  is the voltage rise on  $C_{VSP}$  when the charging phase is completed. In K7315, the  $V_{VSP}$  judges whether the VSP is generated by primary side power switch or not is set by an internal current source  $I_{REF}$  and outside resistor  $R_{REF}$  (R14 in Fig.1). So, the judging volt-second product

$$VSP_{REF} = (R_{VSP} * C_{VSP} * I_{REF}) * R_{REF} = ASP * R_{REF}$$

Where ASP=( R<sub>VSP</sub>\*C<sub>VSP</sub>\*I<sub>REF</sub>) is a K7315 determined "Ampere Second Product" to set system VSP<sub>REF</sub> with R<sub>REF</sub>. VSP<sub>REF</sub> depends on system design and are always fixed after system design is frozen. R<sub>REF</sub> resistor should be considered for the worst case, that is, the minimum primary peak current condition. VSP<sub>REF</sub> should be designed in the middle of VSP1 and VSP2.

If we set

$$VSP_{REF}=25V*\mu S$$

Then

$$R_{REF} = VSP_{REF}/ASP = 36k\Omega$$



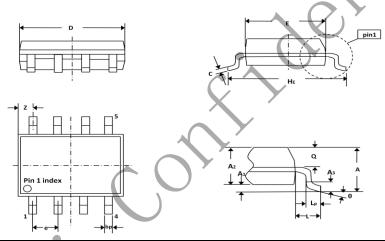
K7315M needs a minimum secondary winding voltage at primary side power switch turn on  $(T_{ONP})$  for SR operation. The value of  $V_{DET}$ –VCC during primary side power switch turn on time  $(T_{ONP})$  must be higher than  $V_{S\_MIN}$ . The corresponding minimum rectified input line voltage  $(V_{IN\_MIN})$  is  $V_{IN\_MIN}$ =  $V_{S\_MIN}$ \* $(N_P/N_S)$ . The resistors in series with DET pin (R12) and VCC pin (R13) are devoted to enhance system ESD and EFT test performance. A 20nF capacitor can be added to the VCC pin of K7315M to filter the noise at the VCC pin during system ESD or EFT test.

### 12. Ordering Information

Part number	Package	Marking ID	Packing	Output power
K7315M	SOP8	7315M	3000/Reel	12W~15W

### 13. Mechanical Dimensions

#### SOP8



UNIT	A	A1	A2	A3	bp	с	D	E	e	HE	L	Lp	Q	θ
mm	1.75	0.1/ 0.25	1.25/ 1.5	0.25	0.33/ 0.51	0.19/ 0.25	<i>4.7/ 5.1</i>	3.8/ 4.0	1.27	5.8/ 6.2	1.05	0.4/ 1.0	0.6/ 0.7	8°

8/8